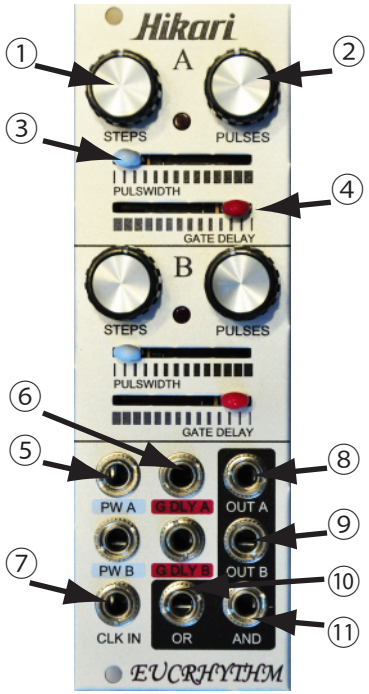
HIKARI EUCRHYTHM MANUAL



HIKARI

EUCRHYTHM

8 HP

35mA: +12V

3mA : -12V

38mm Depth

①STEPS: Sets the loops step length.
Range can be set between 1 - 16.

②PULSES: Sets the number of gates that are output according to the step set in ①.
Number of steps is half when the nob is in center position, and increases as it is turned clockwise.

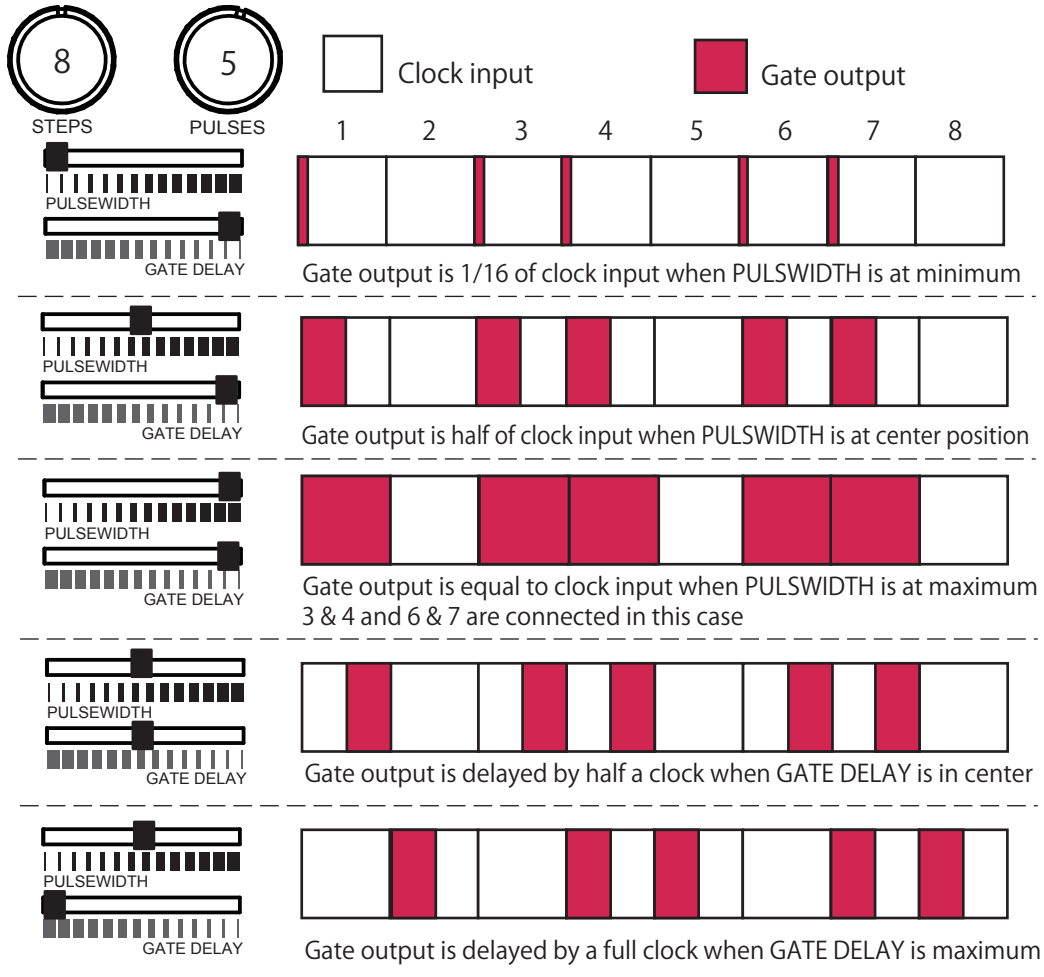
③PULSEWIDTH: Sets the length of the output gate.
Gate length can be changed according to the multiple of a unit proportional to 1/16 of the clock input.
PW is at minimum when set far left, and PW is maximum when set far right.
At minimum, gate width is 1/16 of the input clock;
at center, gate width is half of the input clock;
at maximum, gate width is a whole step width
(if the next step is ON, the gate stays high)

④GATE DELAY: Sets the time of the gate output delay against the clock.
Delay time can be changed according to the multiple of a unit proportional to 1/16 of the clock input.
PW is at minimum when set far right, and PW is maximum when set far left.
At minimum, delay time is 1/16 of the input clock;
at center, delay time is half of the input clock;
at maximum, delay time is a whole step width

⑤PW A: Channel A's PULSWIDTH CV control
When slider is at minimum (slider set fully to the left):
CV input of 0 - 5V modulates gate width from 1/16 of the input clock to full step of the input clock
(anything below 0V or above 5V is ignored)

When GATE DELAY slider is at minimum
(nob turned fully clockwise):
CV input of 0 - -5V modulates gate width from full step of the input clock to 1/16 of the input clock
(anything below -5V and above 0V is ignored)

＜PULSWIDTH, GATE DELAY gate output diagram＞



⑥G DLY A: Channel A's GATE DELAY CV control
When slider is at minimum (slider set fully to the right):
CV input of 0 - 5V modulates delay time from no delay to full step delay of the input clock
(anything below 0V or above 5V is ignored)
When slider is at maximum (slider set fully to the left):
CV input of 0 - -5V modulates delay time from full step delay of the input clock to no delay
(anything below -5V or above 0V is ignored)

⑦CLK IN: Clock input
⑧OUT A: Channel A gate output (10V)
⑨OUT B: Channel B gate output (10V)
⑩OR: Outputs a gate signal when Channel A or Channel B fulfills a logic OR
⑪AND: Outputs a gate signal when Channel A or Channel B fulfills a logic AND

Hikari INSTRUMENTS